

## EE8217 DESIGN PROJECT FORMAT

- 1. Abstract:**  
Brief description of project objectives and results.
- 2. Project Specification:**
  - 2.1** Functional Spec.: description of the function algorithm and data structure.
  - 2.2** Technical Spec.: determination of performance parameters and constrains.
- 3. Theory:**
  - 3.1** Presentation or algorithm in the form of sequencing graph.
  - 3.2** Scheduling and binding with resources according to ASAP timing diagram (to be provided re: Lecture 10 Notes).
  - 3.3** Determination of timing parameters: Latency and Cycle time  $\leq$  Spec. limits
  - 3.4** Determination of types of resources (adders multipliers, LUTs, etc.) and minimum amount of each type of resources to satisfy Spec. requirements.
  - 3.6** Determination of Initiation and Termination Cases and list of associated signals (according to Lecture 10 Notes).
- 4. Design:**
  - 4.1** Creation of the “Symbol” of the Component (with all init/termination inputs, data I/O buses and associated strobes, custom control/feedback signals, clock, enable, reset signals, etc.).
  - 4.2** Conversion of the scheduled and bind graph to the data-path block diagram (including determination of resource multiplexing scheme).
- 5. Implementation:**
  - 5.1** HDL coding with comments (Source code and compilation results to be attached in Appendix “A”).
  - 5.2** C-coding for MicroBlaze or other soft-core processor (Source code and compilation results to be attached in Appendix “B”).
- 6. Verification:**
  - 6.1** Timing simulation and Hardware timing emulation (using ChipScope Pro). with comments for: Init case / Start –up (Latency) / End cycle / Termination case (to be attached in Appendix “A”).
  - 6.2** Timing results for soft-core implementation (to be provided in Appendix B).
- 7. Comparative analysis:**
  - 7.1** Calculation of Speedup.
  - 7.2** Total cost estimation for production series 100, 1000 and 10,000 units.
  - 7.3** CPR = Amount of data processed / sec. per 1\$ for soft-core and ASP (application specific processor) implementation for 100, 1000 and 10,000 units.
- 8. Conclusion**

*Total page limit = 15 pages: Times Roman 12, Single spaced, Figures, Tables included  
Appendices excluded (Appendices are additional pages)*